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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/647,605	08/25/2003	S. Brandon Keller	100111260-1	2817

22879 7590 09/21/2005

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EXAMINER	
DIMYAN, MAGID Y	
ART UNIT	**PAPER NUMBER**
2825	

DATE MAILED: 09/21/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/647,605	KELLER ET AL.	
	Examiner	Art Unit	
	Magid Y. Dimyan	2825	

-- *The MAILING DATE of this communication appears on the cover sheet with the correspondence address* --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 August 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-29* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 August 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *1/20&2/6/04,6/8/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This Office Action pertains to U.S. Patent Application No. 10/647,605, filed on 25 August 2003. Claims 1 – 29 remain pending in this Application.

Specification

2. The disclosure is objected to because of the following informalities:

The U.S. patent application serial numbers of the copending, co-filed applications are missing in paragraph 0001.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1 – 29 are rejected under 35 U.S.C. 102(e) as being anticipated by Pub. No. US 2003/0237067 to Mielke et al. (hereinafter, "Mielke").

5. Pursuant to claims 1, 16 and 23, Mielke discloses a method (claim 1), a system (claim 16) and a computer program (claim 23) for performing circuit analysis on a circuit

design (see Abstract) comprising: determining instantiation paths for one or more design blocks of the circuit design (see Fig. 6; paragraphs 0065-0068 and 0079-0081); recursively accumulate select information for each of the design blocks (see Fig. 6; paragraphs 0065-0068 and 0079-0081); and applying instantiation characteristics to the accumulated information for each instance of the design blocks based upon instantiation hierarchy of the instance within the circuit design (see Figs. 2, 5, 6 and 7; paragraphs 0065 – 0067 and 0079 – 0082). Thus, Mielke cites all the claimed limitations.

6. Regarding claim 10, Mielke teaches a system for performing circuit analysis on a circuit design (see Abstract) comprising: a user interface for selecting one or more design blocks of the circuit design (see Figs. 1 and 2; paragraphs 0027and 0029); an analysis tool operable to determine instantiation paths for the design blocks, accumulate select information for each instance of the design blocks, and applying instantiation characteristics of each instance of the accumulated information (see (5) above); and memory for storing the instantiation paths, the accumulated information, and results based upon the applied characteristics (see Fig. 2; paragraphs 0027 – 0033). Thus, Mielke discloses all the elements, as claimed.

7. As per claims 2, 11, 17 and 24, see Fig. 2, blocks 253 and 256; paragraphs 0035, 0036 and 0056 which cite the claimed elements pertaining to circuit and transistor capacitances.

8. Referring to claims 3, 12, 18 and 25, see Figs. 4A, 4B and 5; paragraphs 0050 – 0055, which teach the limitation of switching frequencies, as claimed.

9. As for claims 4, 13, 19 and 26, see Figs. 6 and 7; paragraphs 0075 – 0081, which recite the claimed step of recursively accumulating selected information for one or more HLSN signal nets within the design blocks (see Fig. 7, block 704).

10. Regarding claims 5 and 6, see Figs. 1 and 2; paragraphs 0027 –0029, which show how a user interface is used to select blocks and HLSNs, as claimed.

11. Pursuant to claims 7 – 9, 14 – 15, 20 – 22 and 27 – 29, see Figs. 3, 5, 6 and 7; paragraphs 0014, 0040 – 0044, and 0066 – 0067, which collectively teach all the claimed limitations pertaining to reading instantiation hierarchy and instantiation characteristics from the circuit design and generating results based upon the instantiation characteristics.

Conclusion

12. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Pub. No. US 2004/0044972 to Rohrbaugh et al. cites a method and apparatus of carrying out an analysis function on a hierarchical circuit model by inputting the model, specifying at least one circuit block within the hierarchy as a target of the function on the target block, and simplifying the model by deleting blocks not affecting the analysis function to produce a simplified hierarchical circuit model.

Pub. No. US 2004/0078767 to Burks et al. discloses a method for modeling IC designs in a hierarchical design automation system that uses a block abstraction that are necessary to achieve accurate placement, routing, extraction, simulation and verification of the block's ancestors in the hierarchy.

US Patent No. 6,587,99 to Chen teaches a method of modeling delays in an IC design that may be used to reduce the computation time of path delays in an IC design which includes the step of approximating effective capacitance of a small net by the total capacitance, and approximating the interconnect delay of the small net by zero.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Magid Y. Dimyan whose telephone number is (571) 272-1889. The examiner can normally be reached on Monday - Friday 8:00 AM - 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew S. Smith can be reached on (571) 272-1907. The fax phone

number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Magid Y Dimyan
Examiner
Art Unit 2825

myd
09 September 2005

A. M. Thompson
Primary Examiner
Technology Center 2800